REMARKS

Applicant recognizes with appreciation that the Examiner indicated that Claims 34 and 37 – 42 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112.

In this Amendment, Applicant has amended Claims 3, 4, 22, 31, 33 – 37 and 42, and added new Claims 43 – 49 to overcome the rejections and specify the embodiments of the present invention. It is respectfully submitted that no new matter has been introduced by the amendment. All claims are now present for examination and favorable reconsideration is respectfully requested in view of the preceding amendments and the following comments.

CLAIMS OBJECTIONS:

Claims 3, 4 and 34 – 37 have been objected as containing informalities. It is respectfully submitted that the informalities have been corrected in the relevant claims. More specifically, in Claim 3, the term *"logic circuit"* has been replaced with *"logic processing circuit"* as suggested by the examiner. The terms *"input interfaces"* and *"output interfaces"* have been replaced by the terms *"at least one digital input interface"* and *"at least one digital output interface"* respectively.

In Claims 4 and 35, the word *"first"* in the term *"said first plurality of logic processing flip-flops"* has been deleted. In Claim 22 and 36, the phrase *"to maintain the level of the output signal(s) to said at least one digital output interface at defined levels, said levels being defined by the levels last sampled"* has been replaced with *"to ensure the output data in the said at least one output register remains unchanged from the output data last stored"* to overcome the Examiner's objection regarding the lack of prior mention of levels of output signals. In Claim 34 and 37, the term *"output registers to be updated"* has been replaced with *"at least one output register"*. The phrase *"maintain the output signal(s) to said at least one digital output interface at the level last sampled*

from the user control program circuit" has been replaced with *"ensure the output data in the said at least one output register remains unchanged from the output data last stored from the user control program circuit when said support circuits were operated according to said second condition".*

The phrase *"enabling said output registers to be updated"* has been replaced with *"enable said at least one output register to be updated".*

New independent claims 43 (based on amended claim 34) and 47 (based on amended claim 37) have been added together with their subsequent dependent claims.

Therefore, withdrawal of the objection is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 112 FIRST PARAGRAPH::

Claims 4, 22, and 33-42 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly failing to comply with written description requirement.

It is respectfully submitted that the currently presented claims have antecedent basis in the specification and satisfy the written description requirement. More specifically, in Claims 4 and 35, the Examiner contends support cannot be found in the specification for a *"first mode"* that operates in the first condition but not in the second condition, and a *"second mode"* that operates in both the first and second condition.

Claims 4 and 35 have been amended. The paragraph *"a monitoring services and control unit arranged to control and operate said logic processing circuit in at least two individually selectable modes of operation, and said logic processing circuit arranged to operate in a continuously repeating logic processing circuit scan cycle, and whereby in a first mode, said monitoring services and control unit is arranged to operate said support circuits in said first condition, to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops, but not in said second condition, whereby in a second mode, said monitoring services and control unit is arranged to operate said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged*

to operate to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops, and when in said second condition said programmable controller is arranged to operate to sample and store the value of at least one input signal from said at least one digital input interface, to apply user clock pulses to said logic processing circuit and to update said at least one output register" has been replaced with *"a monitoring services and control unit arranged to control and operate said logic processing circuit including:*
a continuously cycling logic processing scan at least including said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged to operate to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops; and when in said second condition said programmable controller is arranged to operate to apply user clock pulses to said logic processing circuit and to update said at least one output register".

The amendment is supported in the description including paragraphs [0110] to [0115] of the specification as published:

[0110] The preferred system continuously cycles through a number of well-defined steps that together may be called an LPC scan. In its preferred form, one cycle of the LPC scan consists of the steps of
[0111] 1. sampling all input data, including previous output values that are to be fed back, and storing the values,
[0112] 2. using the stored values as input data for the logic processing circuit, and allowing the circuit to process, and the output data from the circuit settle to a stable value,
[0113] 3. performing tasks on the LPC required for programmable controller monitoring and control, including data transfer and modification,
[0114] 4. transferring the output data from the logic circuit and storing the values on the system output. Allowing the system outputs to settle before repeating
[0115] The steps 1 to 4 above can be thought of as a single logic processing cycle.

Regarding Claim 33, the Examiner contends there is lack of support for *"the flip-flops connected as a shift register have their order in the shift register determined by programmable logic device configuration"*.

Claim 33 has been amended. The phrase *"the flip-flops connected as a shift register have their order in the shift register determined by programmable logic device configuration"* has been replaced with *"said plurality of logic processing circuit flip-flops are interconnected to form a shift register by the programmable device configuration process"*. Support for the amendments is provided in paragraphs [0201] and [0202]:

[0201] Configured Means of Access

[0202] FIG. 9 shows an example of a single LPC 59 arranged to exchange data with an external circuit 62. It is arranged that all of the flip-flops as at 60, configured in the LPC user control program circuit, are interconnected as at 63 to form a shift register. The flip-flops, as at 60, within the LPC are numbered "1" to "8" to show their position in the shift register. The data in any flip-flop may be accessed by shifting it out of the LPC. The number of shift pulses required is calculated from the flip-flop number. The flip-flop number therefore functions as an address.

For Claim 31, the phrase *"operating within said logic processing mode"* has been replaced with *"operating with logic processing enabled"*. Reference to *"pause mode"* has been removed, with the phrase *"switching the mode of said outgoing user program circuit to pause model"* being replaced by *"pausing said outgoing user program circuit"*.

Support for the amendment can be found in the description paragraph [0153]:

[0153] To those skilled in the art, it will be readily apparent from the description in this specification how a user control program can be started, paused, resumed and stopped. Other than saying that these functions may be implemented by suitable logic, sequencing and control of the various system clocks, no further comment will be made. The other aspects will now be dealt with.

The phrase *"switching the mode of said incoming user program circuit to said logic processing mode"* has been replaced by *"restarting said incoming user program circuit, enabling processing of said incoming user program circuit"*.

For Claim 42, the phrase *"placing the non-failing said blocks in pause mode"* has been replaced with *"pausing the non-failing said blocks."* The phrase *"restarting said blocks in said logic processing mode"* has been replaced with *"restarting said blocks by enabling logic processing"*.

Other amendments have been made to correct typographical errors. In light of the above, applicant contends that all terms used in the claims have a clear and unambiguous meaning and are fully supported by the description. Therefore, withdrawal of the rejection is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102:

Claims 3, 4, 22, 33, 35 and 36 have been rejected under 35 U.S.C. § 102 (e) as allegedly being anticipated by How et al. (US 6,611,932), hereinafter HOW.

Applicant traverses the rejection and respectfully submits that the present-claimed invention is not anticipated by the cited references. More specifically, Amended Claim 3 requires "*at least one digital output interface for receiving data from at least one output register*". The required output register of amended Claim 3 is described in at least paragraph [0105] where *"The LPC output values 18 are sampled and stored by the output registers 14 and transferred to the system output terminals 16 via the interface circuits 15"*. The output register facilitates maintaining control of a process or machinery by isolating the FPGA outputs from the random logic levels generated when data is clocked in and out of the logic processing circuit.

HOW describes a method of accessing data in an integrated circuit (IC) suitable for use in testing ICs. How does not disclose "*at least one digital output interface for receiving data from at least one output register*" as required by amended Claim 3.

Thus, Applicant contends that amended Claim 3 is novel and provides a useful system not previously available to the public. As Claims 4, 22, 33, 35 and 36 are dependent upon Claim 3, they are also novel over HOW.

To add further clarification, the object of HOW is to test IC's to prove correct functionality, to prove that the IC as manufactured and processed to date is functional as specified. HOW does not maintain the IC-under-test outputs at levels defined by normal user circuit operation. Rather, the output pins in How will be exposed to random logic levels generated by the internal operation of the test access procedure. This is not a problem if the IC is isolated from other circuitry such as when being tested on a test machine as described. However, it would result in catastrophic malfunction of machinery if it were used for Applicant's purpose.

Applicant's reason for accessing data in an FPGA IC is not to prove that the IC itself is fully functional. Rather it is to allow monitoring and debug of the overall system operation resulting from the data that has been configured into the FPGA to cause the FPGA to operate as a circuit defined by the user. The FPGA IC in Applicant's application must be able to provide access to user circuit state data, and leave it undisturbed, while the IC continues to maintain control over a process or machinery.

It is well-known that ICs may pass tests performed on a test machine, but still fail to work as expected in an application circuit. Such a situation may arise because of errors or omissions in the specification and design process or in testing the IC.

The benefit of the present invention is to be able to 'look inside' the IC while it is operating as part of the application which as a whole fails to perform properly. The ability to monitor and view the internal IC operations makes the diagnosis of the problem much simpler and quicker. In the absence of this ability, the diagnosis must rely on measurements taken at the IC pins. HOW provides no solution to this problem.

Therefore, the presented claims are not anticipated by HOW and the rejection under 35 U.S.C. § 102 (e) has been overcome. Accordingly, withdrawal of the rejections under 35 U.S.C. § 102 (e) is respectfully requested.

REQUEST FOR INTERVIEW:

If the pending claims as presented are not allowable, Applicant respectfully requests the Examiner to contact attorney below to conduct an interview before issuance of an office action, so that prosecution of the application can be advanced towards allowance.

Having overcome all outstanding grounds of rejection, the application is now in condition for allowance, and prompt action toward that end is respectfully solicited.

Respectfully submitted,

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